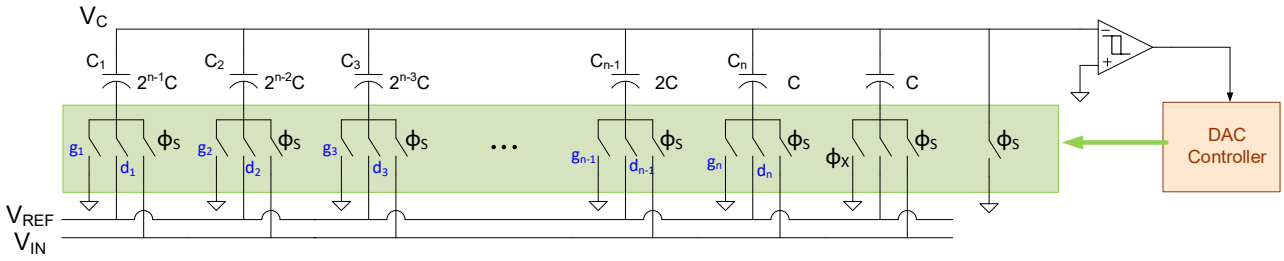
EE 505
Final Exam
Spring 2025
Due at 2:00 p.m. on Wednesday May 14.

Problem 1 A 3-bit DAC designed with a 1V reference had the following outputs. It has been proposed to use this DAC as the DAC in a basic ΔΣ oversampled ADC. How many bits of resolution (ENOB) from a linearity viewpoint (INL) can be expected from the ΔΣ (over-sampled) ADC?

Code	Output
000	3.05176E-05
001	0.12500000
010	0.249992371
011	0.374984741
100	0.500061035
101	0.625030518
110	0.750015259
111	0.87500000

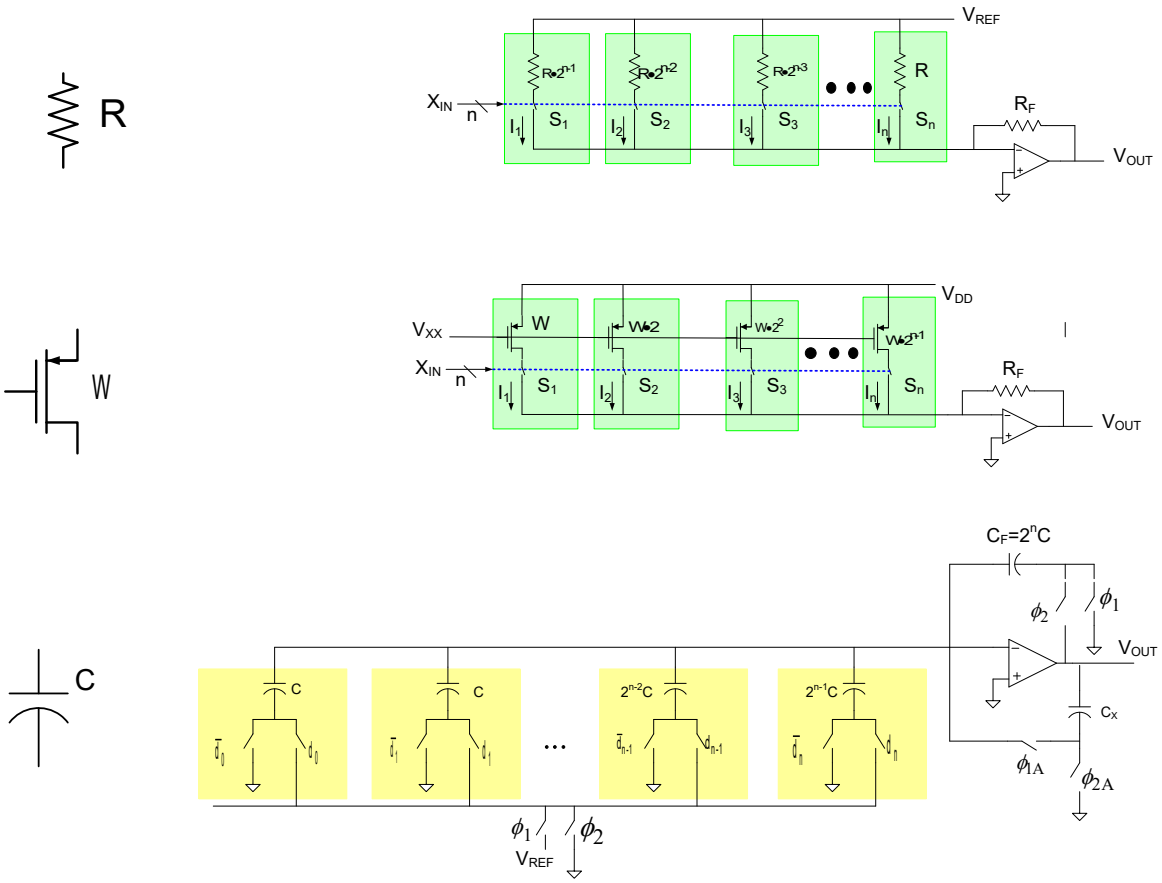
Problem 2 A basic charge-redistribution SAR ADC is shown below. Assume this is designed for 5-bits of resolution and that a binary search algorithm is used in the converter. If V_{REF}=1V, plot the voltage V_C and the comparator output for the conversion of the input signal V_{IN}=0.638V. These should be shown along with all relevant clocking symbols with the same time axis. You may assume all components are ideal and the clock frequency is 1MHz.



Problem 3 The RMS noise voltage on a basic sampled capacitor is $\sqrt{\frac{kT}{C}}$. Thus for a given resolution on a charge redistribution DAC, there is a lower bound on the size of the capacitor if the RMS noise voltage is to be set at the ½ LSB level. Correspondingly, there is a lower bound on the area for the capacitor if the INL of the DAC is set at the ½ LSB level. The capacitor sizing requirements are typically dominated by either the noise or resolution specifications. Determine at what bit-level the sizing requirements for both are the same. Assume the yield is to be at the 99% level and the Pelgrom capacitor matching parameter is A_C=0.015μm. For the purpose of yield calculations, assume the yield is based upon the maximum INL_k parameter rather than the INL parameter since we have closed-form expressions for the maximum INL_k value.

Problem 4 In a given process, there are several different options for implementing the DAC in a SAR ADC. The most common are an R-DAC, a MOS transistor based current-steering DAC, and a charge redistribution DAC. In all 3 cases, there is a unary element and the matching characteristics of the unary element determine the area that is needed for a given linearity yield. The three basic structures are shown below along with the unary elements on the left. Determine the relative area required in all 3 cases for a given yield if they come from a process with the following statistical matching parameters. Though a specific value for the yield is not needed for determining the relative area, you may assume the target yield is 99% if you prefer. Neglect the feedback elements for all 3 cases, assume common centroid layout will be used to eliminate gradient effects, and assume all switches are ideal. (Neglecting the feedback element is justifiable for the resistor and transistor structures but may not be so for the charge-redistribution structure.)

Resistor	Capacitor	Transistor	
A_ρ	A_C	A_β	A_{VT0}
0.1 µm	0.015 µm	0.01 µm	0.02 V·µm
$\sigma^2_{\frac{R_R}{R_N}} = \frac{A_\rho^2}{WL}$	$\sigma^2_{\frac{C_R}{C_N}} = \frac{A_C^2}{WL}$	$\sigma^2_{\frac{\beta_R}{\beta_N}} = \frac{A_\beta^2}{WL}$	$\sigma^2_{V_{THR}} = \frac{A_{VT0}^2}{WL}$



Problem 5 Consider a 2-bit R-string DAC shown below comprised of eight 1KΩ resistors (denoted as unary resistors) with V_{REF}=4V with the same process parameters listed in Problem 4 where the 3 "R" resistors are comprised of the series interconnection of two of the unary resistors and the R/2 resistors are each comprised of a single unary resistor. Assume everything is ideal except for local random variations in the resistor values.

a) Determine the area required for the unary resistors if the DAC is to have a yield of 99% with an INL ENOB of 14 bits.

b) Define $V_{IN}(t) = 2 + 2\sin(100t)$. Determine the RMS noise voltage and the SNR at the output of the DAC due to the thermal noise in the resistors if $X_{IN} = B(V_{IN}(t))$ where B(y) denotes the binary representation of the base 10 number y. Assume samples are taken every 1m sec. Use the resistors determined in part a) for this noise analysis.

c) Determine the nominal value of the unary resistor (which will no longer be 1KΩ) needed to obtain an ENOB from a SNR viewpoint at the 14-bit level (consider only resistor thermal noise in the SNR ratio).

d) How does the area required to obtain a 99% INL yield change if the resistor values determined in part c) are used instead of the 1KΩ resistors?